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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/648,206	08/27/2003	Alfred P. Turley	1215-0485P (000277-078)	3492

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EXAMINER	
LOKE, STEVEN HO YIN	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/648,206	TURLEY, ALFRED P.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) *7-12* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claims 7-12 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 10/1/04.

2. Claim 5 is objected to because of the following informalities: line 3, the phrase "a source and drain region" is unclear whether it is being referred to "a source region and a drain region". Appropriate correction is required.

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Nakagawa et al.

In regards to claim 1, Nakagawa et al. show all the elements of the claimed invention in fig. 32. It is a semiconductor wafer structure, comprising: at least one bipolar transistor (BiTr) defined in said semiconductor wafer structure; at least one CMOS transistor device (nMOS, pMOS) defined in said semiconductor wafer structure; said CMOS transistor device being comprised of a thin film of semiconductor (a first polycrystalline semiconductor layer) on an insulating layer [102]; each transistor of said CMOS transistor device being defined in said thin film and including spaced apart source and drain regions [128Sn, 128Dn, 128Sp, 128Dp] and an intermediate channel region [129p, 129n], each said region being the thickness of said thin film; and a

respective gate [127] disposed on an oxide film [126] on said channel region of each said CMOS transistor device; and a plurality of electrodes [135, 136, 137, 138S, 138D, 139S, 139D] connected to selected elements [131, 133, 125b, 128Sn, 128Dn, 128Sp, 128Dp] of said bipolar transistor and said CMOS transistor device.

In regards to claim 2, Nakagawa et al. further disclose said bipolar transistor includes a base [131]; said base being of a silicon-germanium semiconductor material.

In regards to claim 3, Nakagawa et al. further disclose the thickness of said thin film of semiconductor is no more than 3000 Å (the thickness of the first polycrystalline semiconductor layer can be about 100 nm (1000 Å) (col. 24, line 57 to column 25, line 3).

In regards to claim 4, Nakagawa et al. further disclose the thickness of said thin film of semiconductor is around 1000 Å.

In regards to claim 5, Nakagawa et al. further disclose said CMOS transistor device includes first and second MOS transistors (nMOS, pMOS) each having a source region [128Sn, 128Sp] and a drain region [128Dn, 128Dp] of a different conductivity type than its channel region [129p, 129n].

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakagawa et al. in view of Celler et al.

In regards to claim 6, Nakagawa et al. disclose said insulating layer [102] is on a substrate [101].

Nakagawa et al. differ from the claimed invention by not showing said substrate has a relatively high resistivity of around 1500 ohm-cm, or greater.

Celler et al. show a substrate [21] has a relatively high resistivity of greater than 10 KOhm-cm in a SOI substrate (col. 3, line 66 to col. 4, line 52).

Since both Nakagawa et al. and Celler et al. teach a polysilicon substrate in a SOI substrate, it would have been obvious to have the polysilicon substrate of Celler et al. in Nakagawa et al. because it subjects to less parasitic capacitance (the abstract of Celler et al.).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (571) 272-1657. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sl
October 30, 2004

Steven Loke
Primary Examiner

Steven Loke